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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,853	07/31/2003	Han-Jong Kim	2557-000168/US	1965

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EXAMINER	
WEINMAN, SEAN M	
ART UNIT	**PAPER NUMBER**
2115	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/630,853	KIM, HAN-JONG	
	Examiner	Art Unit	
	Sean Weinman	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on 01 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to the amendment filed on 2 February 2007. ***Claims 1-20*** are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (US Patent Application Publication 2002/0026596) in view of Johnson (US Patent No. 6,859,886).

As per claims 1, 7, and 20, Kim teaches the invention comprising:

a selecting circuit for outputting a selection signal *(Figure 2 Reference 140 and Paragraph [0017] lines 1-5)*;

a high-speed control circuit for controlling high-speed operations in response to the selection signal *(Figure 2 Reference 130 and Paragraph [0014]);* and

a low-speed and low-power control circuit for controlling low-speed and low-power operations in response to the selection signal *(Figure 2 Reference 120 and Paragraph [0015]);* and

a multiplexer for interfacing one of the high-speed control circuit and the low-speed and low-power control circuit *(Figure 2 Reference 160 and Paragraph [0018]).*

Kim, however, does not teach that the selecting circuit determines the operational state of the processor and outputs the selection signal based on the evaluation of the operational state of the processor. Additionally, Kim does not teach that the processor has a processor core and at least one peripheral device. Specifically, Kim teaches a processor with a high-speed control circuit and a low-speed control circuit, a multiplexer that is controlled by a selection signal for selecting either the high-speed or low-speed control circuits.

Johnson teaches a clock control circuit for a processor that monitors and determines the operating state of the processor and then outputs a selection signal to control the processor clock to reduce the power consumed by the processor. Johnson teaches a selecting circuit for determining an operating frequency of the processor and for outputting a selection signal based on the determination *(Col. 3 lines 7-29 and lines 57-67 and Col. 4 lines 1-3).* Additionally, Johnson teaches controlling the clock of a processor core and a peripheral device *(Col. 2 lines 64-67 and Col. 3 lines; CTX0 and CTX1).* In summary, Johnson teaches monitoring and determining the operating state of the processor and then controlling the clock speed of the processor in order to reduce the power consumed and additionally controlling the clock speed of a processor core and peripheral device.

It would have been obvious to one of ordinary skill in the art to combine the teachings of Kim and Johnson because they both teach a processor having a controller unit to control the clock frequency of a processor. Johnson teaches the deficiency of Kim by teaching a selection circuit for determining an operational state and outputting a selection signal based on that determination to control the clock of the processor to reduce the power consumed and controlling the clock of a processor core and peripheral device.

As per claims 2 and 8, Kim and Johnson teach the invention comprising:

Kim teaches the high-speed control circuit controls the high-speed operations of one of at least the processor core and the peripheral device if the operating frequency indicates the processor is operating in a normal mode *(Figure 2 Reference 130 and Paragraph [0014]),* and the low-speed and low-power control circuit controls the low-speed and low-power operations of one of at least the processor core and the peripheral device if the operating frequency indicates the processor is operating in a slow mode *(Figure 2 Reference 120 and Paragraph [0015]).* Johnson teaches the determining whether the processor operating state is in a slow or normal mode *(Col. 3 lines 7-29 and lines 57-67 and Col. 4 lines 1-3).* Additionally, Johnson teaches a processor core, peripheral device and a control circuit controlling the frequency of the processor core and the peripheral device *(Col. 2 lines 64-67 and Col. 3 lines; CTX0 and CTX1).*

As per claims 3 and 9, Johnson teaches the invention comprising:

wherein the selecting circuit compares the operating frequency of the processor with a predetermined threshold frequency and outputs the selection signal based on the compared result *(Col. 3 lines 7-29 and lines 57-67 and Col. 4 lines 1-3).*

As per claim 4, Kim and Johnson teach the invention comprising:

Kim teaches the high-speed control circuit controls the high-speed operations of one of at least the processor core and the peripheral device when the operating frequency of the processor is higher than the predetermined threshold frequency *(Figure 2 Reference 130 and Paragraph [0014]),* and the low-speed and low-power control circuit controls the low-speed and low-power operations of one of at least the processor core and the peripheral device when the operating frequency of the processor is lower than the predetermined threshold frequency *(Figure 2*

Reference 120 and Paragraph [0015]). Johnson teaches the determining whether the processor operating state is operating higher or lower than a predetermined threshold *(Col. 3 lines 7-29 and lines 57-67 and Col. 4 lines 1-3).* Additionally, Johnson teaches a processor core, peripheral device and a control circuit controlling the frequency of the processor core and the peripheral device *(Col. 2 lines 64-67 and Col. 3 lines; CTX0 and CTX1).*

As per claim 5, Johnson teaches the invention comprising:

processor core is a central processing unit (CPU) *(Col. 2 lines 64-67 and Col. 3 lines; CTX0).*

As per claim 10, Kim and Johnson teach the invention comprising:

Kim teaches a circuit for selecting a control circuit from a plurality of control circuits *(Figure 2 and Paragraphs [0014], [0015], and [0017] lines 1-5)*

Johnson teaches selecting based on an operating frequency of a processor *(Col. 3 lines 7-29 and lines 57-67 and Col. 4 lines 1-3)*, the control circuit for controlling one of at least a first device and a second device *(Col. 2 lines 64-67 and Col. 3 lines; CTX0 and CTX1).*

As per claim 11, Kim and Johnson teaches the invention comprising:

Kim teaches an interface device for interfacing the selected control circuit with at least one of the first device and the second device *(Figure 2 Reference character 160).*

Additionally, Johnson teaches a processor core, peripheral device and a control circuit controlling the frequency of the processor core and the peripheral device *(Col. 2 lines 64-67 and Col. 3 lines; CTX0 and CTX1 It would have been obvious to one of ordinary skill in the art that a interface is present for the control circuit to control both CTX0 and CTX1).*

As per claim 12, Johnson teaches the invention comprising:

the circuit for selecting compares an operating frequency of the processor to a threshold value in a process of selecting the control circuit from the plurality of control circuits.

As per claim 13, Kim and Johnson teach the invention comprising:

Kim teaches selecting a first control circuit of the plurality of control circuits when the operating frequency is higher than the threshold value *(Figure 2 Reference 130 and Paragraph [0014])*.

Johnson teaches the determining whether the processor operating state is operating higher than a predetermined threshold *(Col. 3 lines 7-29 and lines 57-67 and Col. 4 lines 1-3)*.

As per claim 14, Kim and Johnson teach the invention comprising:

Kim teaches selecting a second control circuit of the plurality of control circuits when the operating frequency is lower than the threshold value *(Figure 2 Reference 120 and Paragraph [0015])*.

Johnson teaches the determining whether the processor operating state is operating higher than a predetermined threshold *(Col. 3 lines 7-29 and lines 57-67 and Col. 4 lines 1-3)*.

As per claim 15, Johnson teaches the invention comprising:

the circuit for selecting evaluates a mode of the processor in a process of selecting the control circuit from the plurality of control circuits *(Col. 3 lines 7-29 and lines 57-67 and Col. 4 lines 1-3)*.

As per claim 16, Kim and Johnson teaches the invention comprising:

Kim teaches selecting a first control circuit of the plurality of control circuits when the mode is a normal mode *(Figure 2 Reference 130 and Paragraph [0014])*.

Johnson teaches the determining whether the processor operating state is in a normal mode *(Col. 3 lines 7-29 and lines 57-67 and Col. 4 lines 1-3).*

As per claim 17, Kim and Johnson teaches the invention comprising:

Kim teaches selecting a second control circuit of the plurality of control circuits when the mode is a slow mode *(Figure 2 Reference 130 and Paragraph [0014]).*

Johnson teaches the determining whether the processor operating state is in a slow mode *(Col. 3 lines 7-29 and lines 57-67 and Col. 4 lines 1-3).*

As per claim 18, Kim teaches the invention comprising:

control circuits includes at least a high-speed control circuit and a low-speed and low-power control circuit *(Figure 2 Reference 130 and 120 and Paragraph [0014] and [0015]);*

As per claim 19, Johnson teaches the invention comprising:

the first device is a processor core and the second device is a peripheral device *(Col. 2 lines 64-67 and Col. 3 lines; CTX0 and CTX1).*

Claims 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (US Patent Application 2002/0026596) in view of Johnson (US Patent No. 6,859,886) and in further view of Applicant's Admission of Prior Art (AAPA).

As per claim 6, Kim and Johnson teach the claimed invention for the all the reasons stated above. Kim and Johnson do not teach that the peripheral device is a wireless LAN card, a PC card, and a liquid crystal display. Specifically, Kim and Johnson teach a processor with a high-speed control circuit and a low-speed control circuit, a multiplexer that is controlled by a selection signal for selecting either the high-speed or low-speed control circuits based on the operating state of the processor.

The AAPA teaches a processor having a processor core, peripheral device and a control circuit controlling the frequency of the processor core and the peripheral device. The AAPA teaches the peripheral device is at least one of a wireless LAN card, a PC card, and a liquid crystal display (LCD) *(Figure 1 Prior Art and Paragraphs [0006] and [0009]).* In summary, the AAPA teaches that the peripheral device is a wireless LAN card, a PC card, and a liquid crystal display (LCD).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Kim and the AAPA because they both teach a processor having a controller unit to control the clock frequency of a processor. The AAPA teaches the deficiency of Kim by teaching that the control unit also controls a peripheral device that is a wireless LAN card, a PC card, and a liquid crystal display (LCD).

Response to Arguments

Applicant's arguments filed on 2 February 2007 have been fully considered but they are not persuasive.

Applicant argues that the operating frequency is adjusted in response to the I/O request count, and is not a determining factor in determining whether to adjust the operating frequency. Johnson teaches that the operating frequency can be adjusted based on a determination of the number of outstanding I/O requests *(Col. 3 lines 8-14).*

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sean Weinman whose phone number is (571) 272-2744. The examiner can normally be reached on Monday-Friday from 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (571) 272-3667. The fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sean Weinman
Examiner
Art Unit 2115